REMARKS

Claims 19-34 were pending in the application before this Office Action. Claims 19, 24, 25, and 29 have been amended in this Response. Claims 19-34 are pending.

All amendments are made in a good faith effort to advance the prosecution on the merits. Applicants reserve the right to subsequently take up prosecution on the claims as originally filed in this or appropriate continuation, continuation-in-part and /or divisional applications.

Claim Objections

Claim 19 was objected to in the office action due to informalities. In response, Applicants have amended claim 19 to correct the identified informalities.

Rejections under § 112

Claims 24, 25, and 29-34 were rejected under § 112 due to insufficient antecedent basis. In response, Applicants have amended claims 24, 25, and 29 to provide antecedent basis.

Rejections under § 102

Claims 19-26 and 28 were rejected under 35 U.S.C. § 102(b). The Office Actions states that:

> 12. Claims 19-26 and 28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel).
>
> 13. Referring to claim 19, Intel has taught a method of shifting a multi-word value comprising:
>
> a. performing a first shift operation on a first portion of the multi-word value to produces one or more overflow bits (Pages 4-16 and 4-17, Bits are shifted out of the source register.);
>
> b. performing a second shift operation on a second portion of the multi-word value,
>
> c. where the second shift operation comprises:

> i. producing a shift result; and concatenating the shift result and the overflow bits (Pages 4-16 and 4-17, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.).

Office Action, pages 3-4.

Applicants respectfully disagree. The double-shift instructions discussed in Intel at 4-16 and 4-17 do not include "a first shift operation" and "a second shift operation" as required by claim 18. The double-shift operations of Intel, by contrast, include only a single shift operation where "[b]its shifted out of the source operand fill empty bit positions in the destination operand, which also is shifted." Intel, 4-16. The double-shift instructions discussed in Intel therefore only include a subset of the method of claim 18. Because Intel does not disclose each element of claim 18, the claim is not anticipated. Each of claims 21-26 and 28 depend from claim 20, and are similarly not anticipated by Intel. Applicants therefore respectfully request withdrawal of the rejections of claims 20-26 and 28.

Rejections under § 103

Claims 27 and 29-34 were rejected under 35 U.S.C. § 103(a) as unpatentable over Intel and U.S. Patent No. 6,314,200 to Silverbrook.

First, claim 27 depends from claim 18, which Applicants have shown to be patentable above. Applicants therefore respectfully request the withdrawal of the rejection of claim 27.

> The Office Action states that:
>
> 25. Referring to claim 29, Intel has taught a processor for processing multi-precision shift instructions, comprising:
>
> a. a program memory for storing instructions including at least one multi-precision shift instruction (Page 3-2, lines 1-3);
>
> b. a program counter for identifying current instructions for processing (page 3-15, section 3.3.5, Instruction Pointer), and
>
> c. a barrel shifter for executing shift instructions (Page 4-16 and 4-17), including the at least one multi-precision shift

instruction (Pages 4-16 and 4-17, SHLD and SHRD), the barrel shifter including:

i. one or more carry registers for storing values shifted out of sections of the barrel shifter (Page 4-16 and 4-17, CF); and logic for concatenating values stored in one or more carry registers with values in the barrel shifter (pages 25-289 to 25-292); and

d. where the barrel shifter is operable to shift a multi-word value (Pages 4-16 and 4-17, SHLD and SHRD shift doubleword operands), and where when shifting a multi-word value the barrel shifter:

1. executes at least one shift instruction to:

(1) load a first operand into a section within the barrel shifter, where the first operand is a first portion of the multi-word value (Pages 4-16 and 4-17, The source operand is loaded into the source register.); and

(2) generate one or more overflow bits (Pages 4-16 and 4-17, Bits are shifted out of the source register.); and

e. executes at least one multi-precision shift instruction fetched from the program memory (Pages 4-16 and 4-17, The SHRD and SHLD instruction are executed.) to:

i. load a second operand into a section within the barrel shifter, where the second operand is a second portion of the multi-word value (Pages 4-16 and 4-17, The destination operand is loaded into the destination register.);

ii. shift the operand; concatenate the operand with one or more of the overflow bits (Pages 4-16 and 4-17, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.); and

iii. output the shifted value (Pages 4-16 and 4-17, The result is stored back into, or output to the destination operand.).

Office Action, pages 3-4.

Applicants respectfully disagree and contend that the combination of Intel and Silverbrook, assuming such a combination were possible, fails to teach each of the elements of claim 29. Claim 29 requires "execut[ing] at least one shift instruction" and "execut[ing] at least one multi-precision shift instruction." The double-shift operations of Intel, by contrast, include only a single shift operation where "[b]its shifted out of the source operand fill empty bit

positions in the destination operand, which also is shifted." Intel, 4-16. The double-shift instructions discussed in Intel therefore only include a subset of the method of claim. Because the combination of Intel and Silverbrook does not disclose each element of claim 29, the claim is not obvious over the combination of references. Each of claims 30-34 depend from claim 29, and are similarly not obvious over the combination of Intel and Silverbrook. Applicants therefore respectfully request withdrawal of the rejections of claims 30-34.

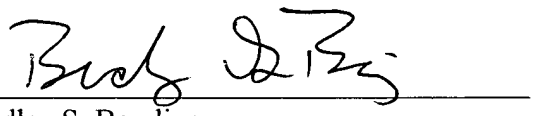
SUMMARY

Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone or facsimile.

Applicants believe that no fees are due at this time. If the Commissioner deems any additional fee is due, the Commissioner is hereby requested to accept this as a Petition therefore, and is authorized to charge any fees due, including any fees for an extension of time, to Baker Botts L.L.P. (formerly, Baker & Botts, L.L.P.) Deposit Account number 02-0383, Order number 068354.1439.

Respectfully submitted,

BAKER BOTTS L.L.P. (031625)



Bradley S. Bowling
Reg. No. 52,641
Baker Botts L.L.P.
910 Louisiana
Houston, Texas 77002
Telephone: (713) 229-1802
Facsimile: (713) 229-7702
ATTORNEY FOR APPLICANTS

Date: November 30, 2005